IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 4. (Cancelled)

5. (New) A nonvolatile memory comprising:

a plurality of input/output terminals; and

a control circuit,

wherein said control circuit is capable of receiving an arbitrary one of a plurality of commands via said plurality of input/output terminals,

wherein said plurality of commands comprise a first type format command and a second type format command,

wherein said first type format command includes a first type command without a second type command,

wherein said second type format command includes said first type command and said second type command,

wherein said first type command indicates an arbitrary one of a plurality of operations, and

wherein said second type command indicates a termination of said second type format command.

6. (New) A nonvolatile memory according to claim 5,

wherein said control circuit is capable of receiving an address information after receiving said first type command, when receiving said first type format command, and

wherein said control circuit is capable of receiving said address information and data after receiving said first type command and before receiving said second type command, when receiving said second type format command.

7. (New) A nonvolatile memory according to claim 6,

wherein said first type format command includes a first read command, a first write command and an erase command, and

wherein said second type format command includes a second write command.

8. (New) A nonvolatile memory according to claim 7, further comprising a nonvolatile memory array and a latch circuit.

9. (New) A nonvolatile memory according to claim 8,

wherein said control circuit controls outputting data read out from said nonvolatile memory array according to said address information when receiving said first read command.

10. (New) A nonvolatile memory according to claim 8,

wherein said control circuit controls writing data stored in said latch circuit to said nonvolatile memory array according to said address information when receiving said first write command.

11. (New) A nonvolatile memory according to claim 8,

wherein said control circuit controls erasing data stored in said nonvolatile memory array according to said address information when receiving said erase command.

12. (New) A nonvolatile memory according to claim 8,

wherein said control circuit controls writing data received from outside to said nonvolatile memory array according to said address information when receiving said second write command.